REMARKS

Claims 1-35 and 37-39 remain pending in the application, with claims 1-29 and 34 having been withdrawn from consideration. Claim 36 has been canceled without prejudice or disclaimer, and Figures 1, 13, 14, 15, 16, 17, 18, 19, 21, 22, 26, 28, and 29 as well as claims 30-33, 35, and 37-39 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

Figures 1, 13, 14, 15 16, 17, 18, 19, 21, 22, 26, 28, and 29 were objected to as failing to comply with 37 CFR §1.84(p)(5) because they include reference signs not mentioned in the description. In addition, Figure 13 was also objected to as failing to comply with 37 CFR § 1.84(p)(4) because:

- the reference character "A" has been used to designate both "start" in Figure 13 and "assign initial stack positions" on page 17, lines 15-17;
- the reference character "B" has been used to designate both "assign initial stack positions" in Figure 13 and "receive respective transaction requests" on page 17, lines 22-23; and
- the reference character "C" has been used to designate both "receive transaction request" in Figure 13 and "determine highest priority level" on page 17, lines 28-30.

In response, Figures 1, 14, 15 16, 17, 18, 19, 21, 22, 26, 28, and 29 have been amended to remove the reference signs identified in the Office Action.

With respect to Figure 13, this has been amended to delete the reference sign "A" from the block labeled "START", and to re-label the blocks "B", "C", and "D" as "A", "B", and "C", respectively. This cures the defect of reference sign "D" not being mentioned in the specification. This amendment also cures the above-mentioned defect of having some reference signs referring to one thing in the figure and another thing in the description. As to reference sign "H" in Figure 13, the Office's attention is directed to the specification at page 18, lines 12-13, where this reference sign is already mentioned. Thus, no further amendment is necessary.

In view of the foregoing amendments and remarks, the figures are believed to be in compliance with the standards set forth in 37 CFR §§1.84(p)(4) and 1.84(p)(5). Accordingly, it is respectfully requested that the objection to the figures be withdrawn.

Claims 30, 31, 33, 35, and 39 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over "The Universal Serial Bus Specification", Revision 1.0 ("USB") in view of IEEE Standard 1394-1995 ("IEEE-1394") and US Patent Number 4,709,364 to Hasegawa et al. ("Hasegawa"). These rejections are respectfully traversed.

Claims 30-33, 35, and 37-39 have been amended to now define "An integrated circuit" rather than an "apparatus"; and claim 39 now defines "A method of granting bus access to a module in an integrated circuit for a computer system." This amendment is supported at various places in the specification, such as at page 10, lines 1-9. Claim 36 is now canceled without prejudice or disclaimer.

It is well established that establishing a *prima facie* case of obviousness requires that three basic criteria be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See MPEP §2143, p. 2100-129 (Rev. 2, 2004).

In the present instance, the Office has failed to make out a *prima facie* case of obviousness against claims 30-33, 35, and 37-39 at least because neither the references relied upon in the rejection nor the knowledge generally available to one of ordinary skill in the art provide any suggestion or motivation to make the combination of their respective teachings. Instead, the Office has engaged in an impermissible hindsight analysis, "us[ing] the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). The Court of Appeals for the Federal Circuit has stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Furthermore, the references relied upon in the rejection relate to different types of bus architectures, so that one of ordinary skill in the art would not have had a reasonable expectation of success in making the combination now suggested by the Office.

These and other arguments are elaborated upon in the following discussion.

Various embodiments of the invention are concerned with bus access to a bus provided on an integrated circuit. In the embodiments, the bus is a pipelined packet switched

bus. In one aspect, two types of arbitration are used: central arbitration is used to allocate timeslots in response to specific requests from agents connected to the bus, and distributed arbitration is used to allow bus access by agents on an ad hoc basis using empty timeslots.

Accordingly, independent claim 30 defines an integrated circuit for a computer system comprising a bus architecture; a plurality of modules connected to the bus architecture; and an arbitration unit for granting access to the bus in response to requests received from the modules, the granting of access being in the form of a dedicated packet issued from the arbitration unit, whereby only the module which has been granted access can use that particular dedicated packet to gain access to the bus. The integrated circuit is characterized in that "the arbitration unit is operable to issue empty packets during periods when the bus is idle, the empty packets being usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet."

Independent claim 39 defines a method of granting bus access to a module in an integrated circuit for a computer system comprising a plurality of modules interconnected by the bus, and an arbitration unit for granting access to the bus by issuing dedicated packets in response to requests received from the modules. As stated in claim 39, the method comprises "issuing empty packets from the arbitration unit during periods when the bus is idle; and allowing any module to use the empty packet in order to gain access to the bus."

In rejecting claims 30-33, 35, and 37-39, the Office relies in part on the USB reference, but acknowledges that this reference at least fails to "teach that the arbitration unit grants access to the bus in response to requests received from the modules; and that the arbitration unit is operable to issue empty packets during periods when the bus is idle, the empty packets being usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet."

To make up for these deficiencies of the USB reference, the Office relies in part on IEEE-1394 for its teaching of "an arbitration unit granting access to the bus in response to requests received from the modules," but here acknowledges that IEEE-1394 also fails to disclose at least "sending an empty packet during periods when the bus is idle that are usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet." To make up for this last missing piece of the puzzle, the Office further relies on Hasegawa as teaching "sending an empty packet during periods when the

bus is idle that are usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet."

The Office's reliance on this combination of references is unfounded because the USB and 1394 documents disclose serial system buses, which are not suitable for use on an integrated circuit. Both systems make use of a global arbitration system which operates to allow or disallow access by all of the agents connected to the bus at the same time. Such techniques are simply not applicable to a packet switched pipeline bus, as used in embodiments of the present invention.

Moreover, the Hasegawa document concerns a token ring packet switched system which has no central arbitration system. In Hasegawa, access to the bus is controlled by the use of empty packets circulating in the ring which are picked up by agents requiring access to the bus. The techniques used in Hasegawa are not applicable to a pipeline bus embodying the subject matter defined by claims 30 and 39, since such a pipeline bus does not allow circulating empty packets. No such central arbitration is possible in the Hasegawa disclosure, since using central arbitration would mean that the ring is broken, or that each agent would be connected to the arbiter independently of one another. Such independent connection would defeat the object of the token ring scheme which is intended to minimize the number of connections.

In making its rejection, the Office uses the approach of starting with the USB document and adding teachings from the IEEE 1394 and Hasegawa documents to derive the invention. However, there is simply no suggestion or motivation provided in any of these references to combine their teachings because all three documents are not relevant to on-chip pipeline buses, and, furthermore, the Hasegawa document is not relevant to the USB and IEEE 1394 documents. It is therefore inconceivable that the person of ordinary skill would combine Hasegawa with either of the other two documents. Hasegawa does not make use of central arbitration, and USB and IEEE 1394 do not use free packets for ad hoc arbitration. The teachings of these three documents would simply not be combined by one of ordinary skill in the art.

Even assuming that the Office were to maintain that the three documents could be theoretically combined, this would be impossible for one of ordinary skill in the art for the following reasons. Starting with the serial system bus of USB, the Office admits that this disclosure teaches neither the provision of access to the bus in response to requests nor the

use of empty packets to allow ad hoc bus access. Although it is not suggested by these references, combining the access on request feature from IEEE 1394 with USB might be possible, since both documents relate to serial system bus designs using global arbitration.

However, Hasegawa proposes control of a token ring network which makes no use of global arbitration, but rather uses a system in which connected agents seize available time slots. There is simply no suggestion that the teaching of Hasegawa is appropriate for use in a serial system bus such as described in USB/IEEE 1394. There is no equivalent mechanism in USB to which to apply the teaching of Hasegawa. To be able to apply such teaching it would be necessary to provide packet switching and timeslot allocation. It is respectfully submitted that such provision goes far beyond normal design practice for one of ordinary skill in the art.

The Office considers the disclosures to be relevant to "on-chip" buses because there are examples of USB controllers "on-chip". (See the Office's argument in paragraph 11 of the Action, made with respect to now-canceled claim 36.) However, the controller simply allows an IC to communicate with an external bus, and the provision of the bus itself on an IC is not a trivial modification. The USB/1394/Hasegawa buses are not intended or appropriate for an on-chip usage.

In USB and IEEE 1394, the arbitration decision is final; no further access is allowed outside of the arbiter's control. In contrast, the present invention allows subsequent ad hoc access, outside of the direct control of the arbiter.

For at least the foregoing reasons, independent claims 30 and 39 are patentably distinguishable over the USB, 1394 and Hasegawa documents, regardless of whether these documents are considered individually or in any combination. Claims 31, 33, and 35 each depend from independent claim 30, and are therefore patentable for at least the reasons set forth above with respect to that base claim. Therefore, it is respectfully requested that the rejection of claims 30, 31, 33, 35 and 39 under Section 103 be withdrawn.

Claim 32 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over USB, IEEE-1394, and Hasegawa as applied to claim 30, and further in view of US Patent Number 5,400,334 to Hayssen ("Hayssen"). Claim 36 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over USB, IEEE-1394, and Hasegawa as applied to claim 30, and further in view of US Patent Number 6,232,932 to Thorner ("Thorner"). Claim 37 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over USB, IEEE-1394, and Hasegawa as applied to claim 30, and further in view of US Patent Number 5,912,710 to

Fujimoto ("Fujimoto"). Claim 38 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over USB, IEEE-1394, and Hasegawa as applied to claim 30, and further in view of US Patent Number 5,986,644 to Herder et al. ("Herder"). These rejections are respectfully traversed.

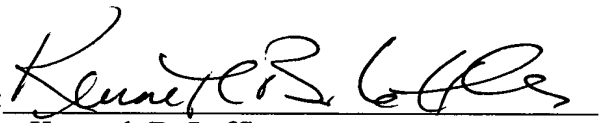
The rejection of claim 36 has been rendered moot by the cancellation of this claim, without prejudice or disclaimer.

The remaining claims each depend from independent claim 30, and are therefore patentably distinguishable over the prior art of record at least for the reasons set forth above with respect to that base claim. Therefore, it is respectfully requested that the rejection of these claims under Section 103 be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
Potomac Patent Group PLLC

Date: November 22, 2004

By: 
Kenneth B. Leffler
Registration No. 36,075

P.O. Box 855
McLean, Virginia 22101-0855
703-718-8884

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on November 22, 2004.


Kenneth B. Leffler, Reg. No. 36,075

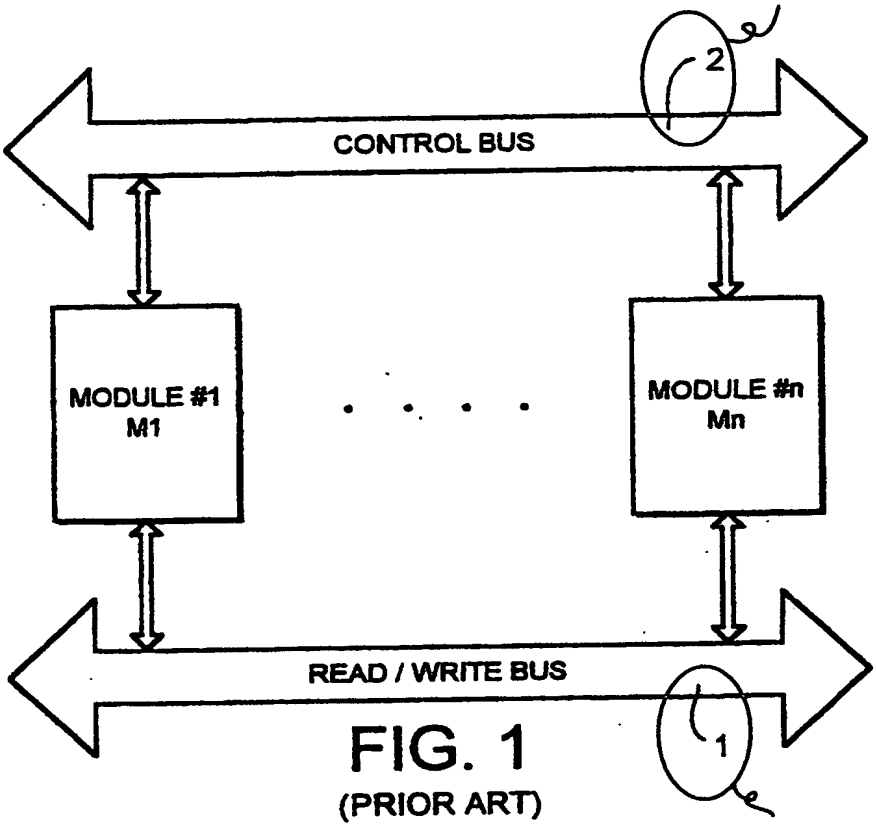


FIG. 1
(PRIOR ART)

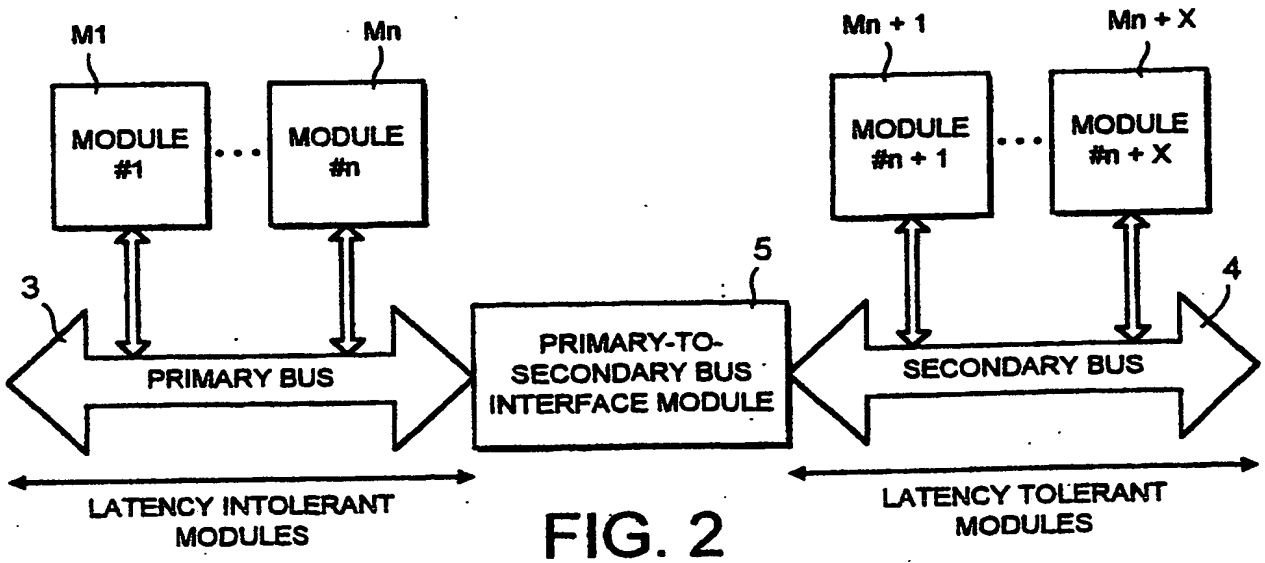


FIG. 2

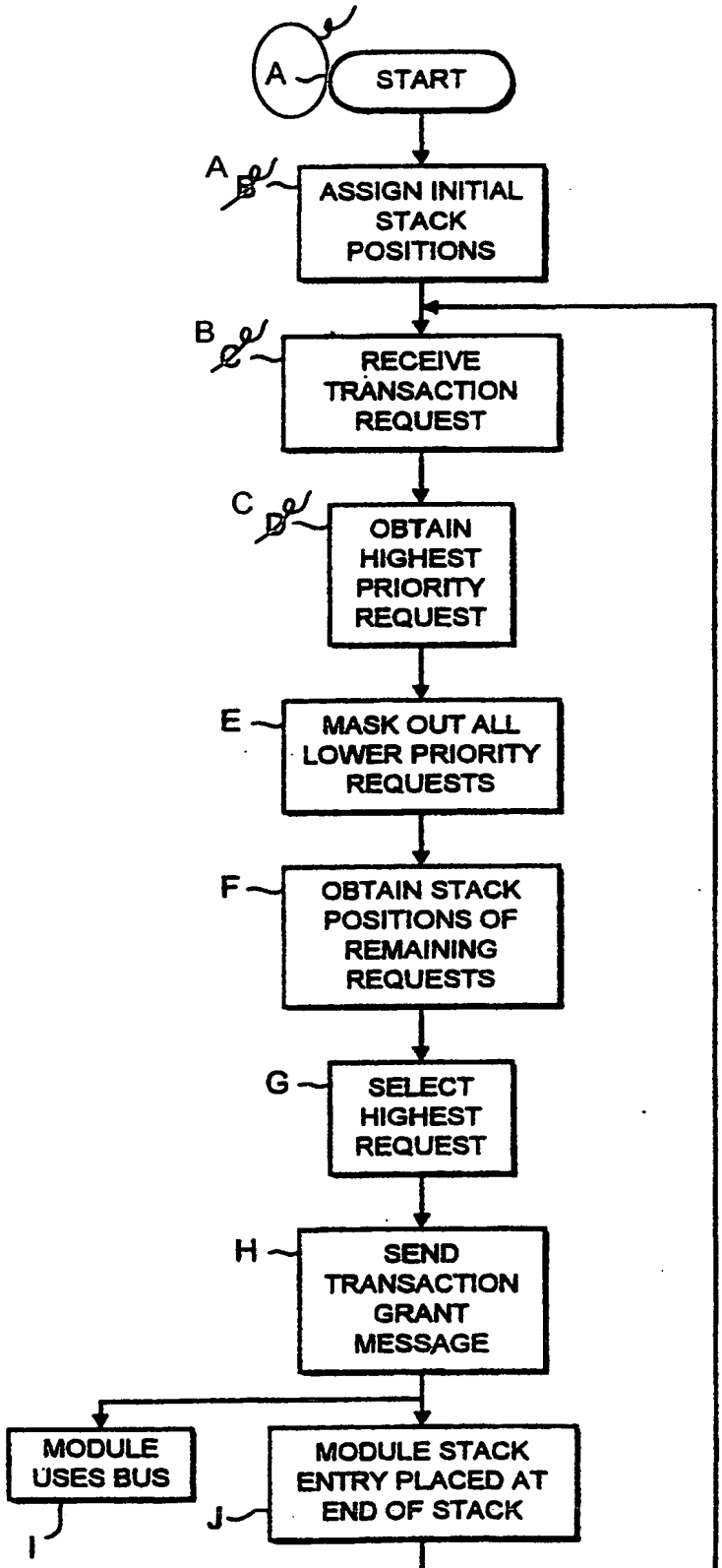


FIG. 13

28 29

MODULE	PRIORITY
M1	H
M2	M
M3	L
M4	H
M5	M

FIG. 14

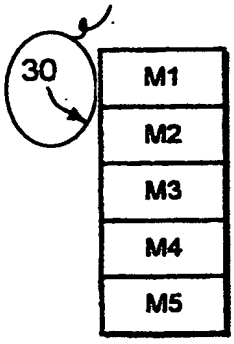


FIG. 15

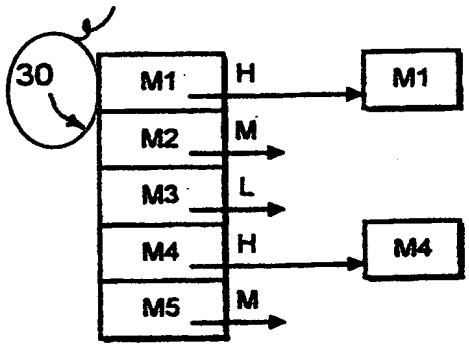


FIG. 16

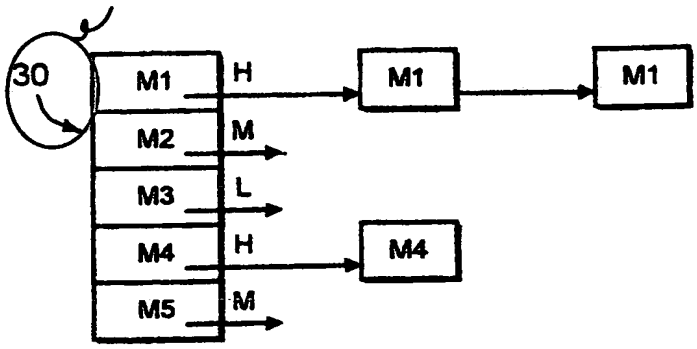


FIG. 17

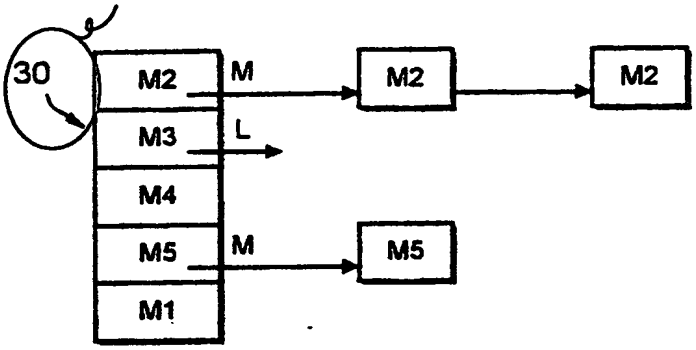


FIG. 18

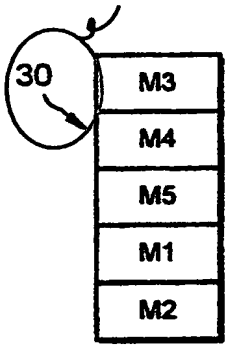


FIG. 19

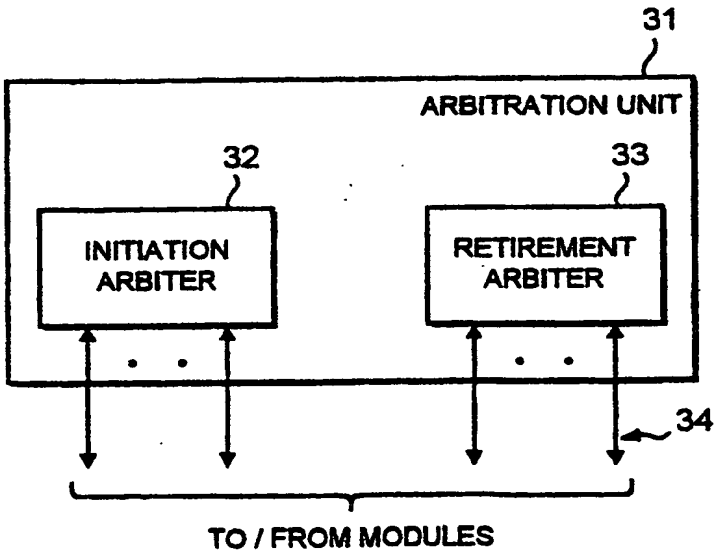


FIG. 20

35 T	R1	W1	R2	W2	R3	W3	....	
36 W		W1A	W1B	W2A	W2B	W3A	W3B	....
37 R				R1A	R1B			
TIME	t	t	t	t	t	t	t	

FIG. 21

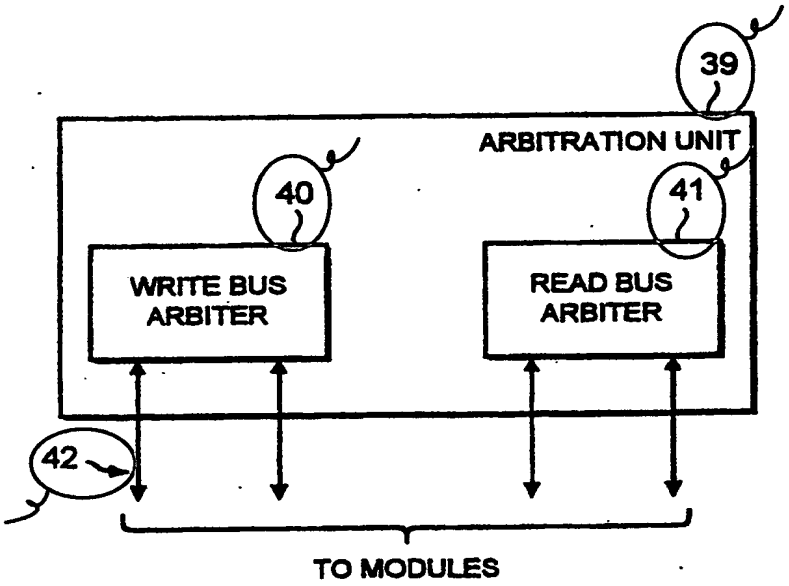


FIG. 22

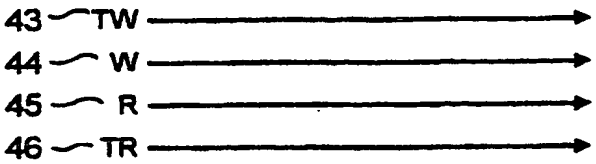


FIG. 23

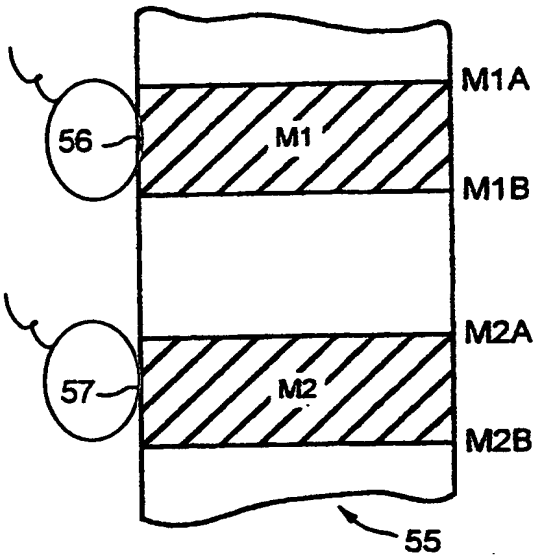


FIG. 26

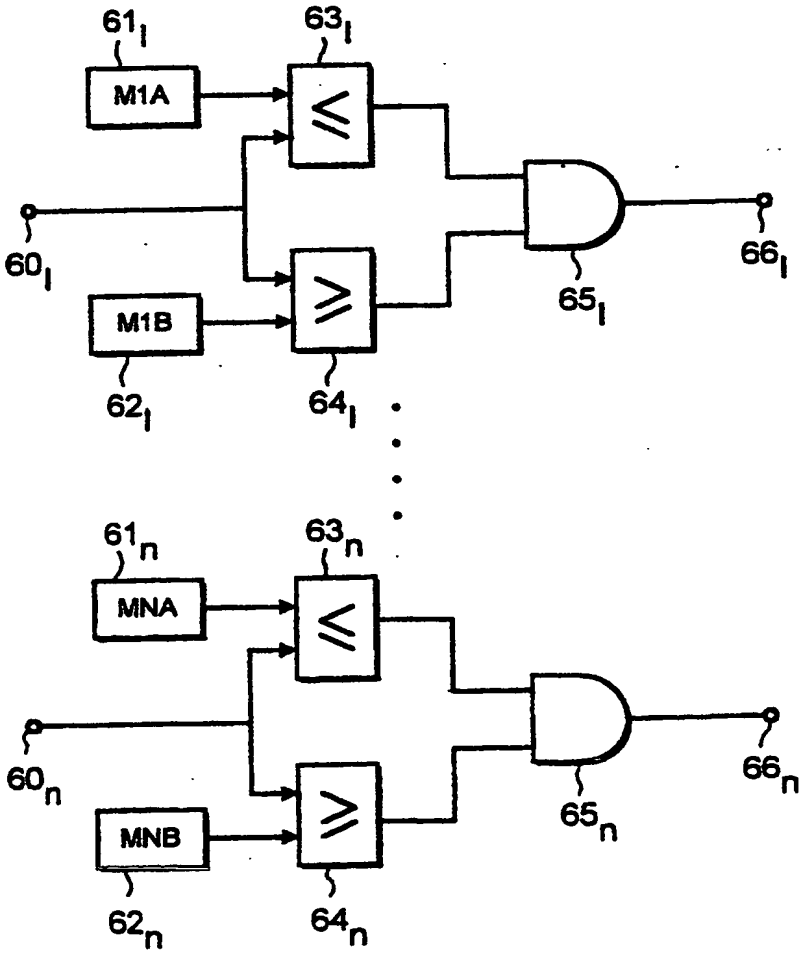


FIG. 27

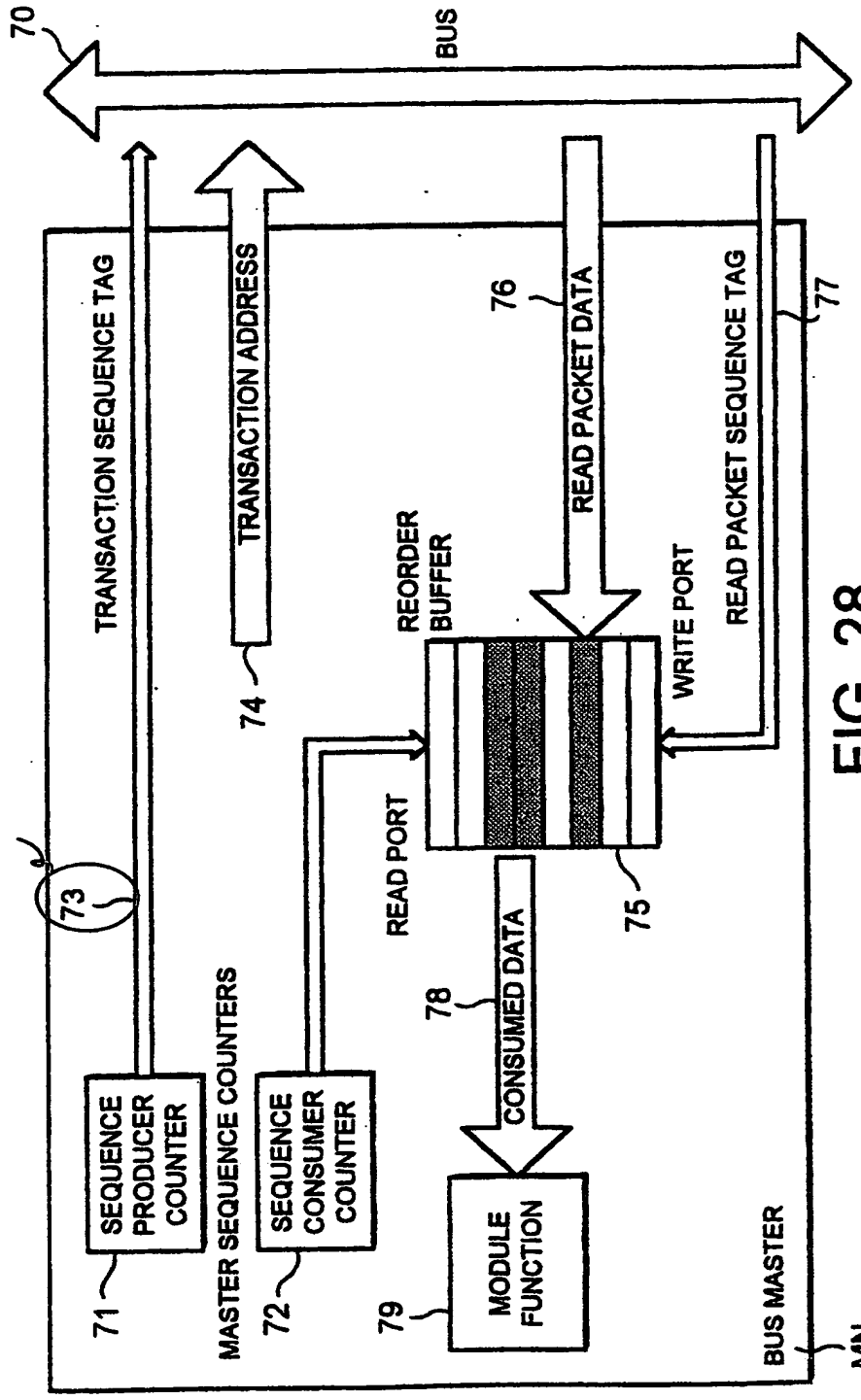


FIG. 28

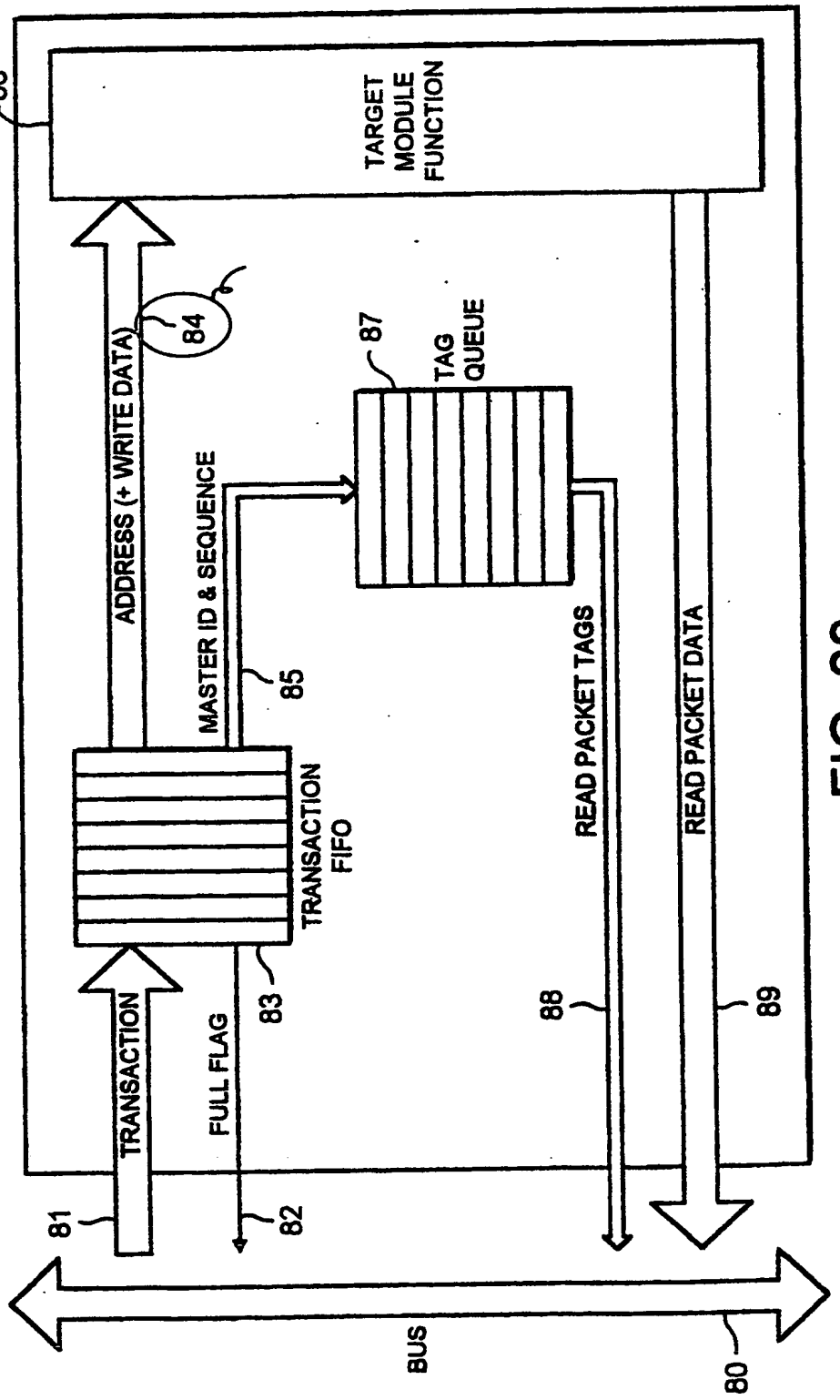


FIG. 29